UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,816	02/05/2004	Aaron J. Barber	BCS03472	5955

43471 7590 12/18/2008

Motorola, Inc.
Law Department
1303 East Algonquin Road
3rd Floor
Schaumburg, IL 60196

EXAMINER	
FEATHERSTONE, MARK D	
ART UNIT	**PAPER NUMBER**
2423	

NOTIFICATION DATE	DELIVERY MODE
12/18/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Docketing.US@motorola.com

Office Action Summary	Application No.	Applicant(s)	
	10/772,816	BARBER ET AL.	
	Examiner	Art Unit	
	MARK D. FEATHERSTONE	2423	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Amendment

Response to amendment filed 11/05/2008. Claims 1, 2, 11-12, 18, and 21-23 have been amended. Claims 1-25 are pending.

Response to Arguments

Applicant's arguments with respect to claims 1-8 and 18-25 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments with respect to claims 9-17 have been fully considered but they are not persuasive. Applicant argues that Farrand, Johnson, and Chaney, in combination teach a first FPGA communicatively coupled to said demodulator or communicatively coupled to said decoder. Examiner respectfully asserts that Johnson does establish the use of an FPGA which is coupled to an MPEG decoder (paragraph [0031]. In the system of Johnson, the FPGA is programmed to forward A/V data to an MPEG encoder/decoder for compression or decompression. As stated in the office action, the system of Farrand discloses the use of a demodulator which is coupled to an MPEG decoder. It would have been obvious to one of ordinary skill in the art to include the well known flexibility of a field programmable device such as the FPGA to transfer the data from the demodulator to the decoder through the use of the FPGA interface, which can provide processing instructions for the data as disclosed in paragraph [0031] of Johnson. In combination, the references of Farrand, Chaney, and Johnson do

render obvious the use of an FPGA that is coupled to a demodulator and decoder.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 22-25 are rejected because the claimed invention is directed to non-statutory subject matter. The claims are directed to a processor readable medium, which could be embodied by a signal or carrier wave. In order to be statutory, a processor readable medium must be embodied as a physical medium which stores instructions. Neither the claims nor applicant's specification limits the processor readable medium to a physical storage medium only.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

   (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4, 22, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farrand, US Patent # 7391808, hereafter Farrand, in view of Hirata, US Patent # 7230734, hereafter Hirata, in further view of Brosnon, US PG Pub # 20040048668, hereinafter Brosnon.

With regard to claim 1, Farrand discloses a method comprising:

Communicatively coupling a removable upgrade decoder to a consumer premise component (CPC), said upgrade decoder being configured to decode a data stream (Figure 1, item 200 illustrates a STB (Set Top Box), corresponding to a CPC; item 300 and column 2, lines 25-34; Farrand describes a module (300) that transcodes media content that is encoded according to a new compression standard). Further, Farrand describes that the module is connected via a USB or P1394 interface (column 3, lines 53-63) corresponding to the module being removable from the system. In contrast, Farrand describes an embodiment (Figure 4) in which the extra decoder is not removable, rather part of the STB.

Although it is well-known in the art that computer code (driver) is needed to access a peripheral device, Farrand does not specifically disclose one.

Hirata, in an analogous art dealing with attaching a device (in this case a printer), does disclose downloading a driver for the device via the cable head end. Such a driver, as is known in the art, would allow the STB to access the device (Figure 2, item 211 printer is attached to item 104 receiver; column 12, lines 4-7; Hirata describes downloading a driver for a device).

It would have been obvious to one of ordinary skill in the art at the time of invention to add the feature of downloading a driver to a CPC as discloses by Hirata to the system of connecting an external decoder to a CPC as taught by Farrand. The advantage would have been to allow the CPC to access the

decoder properly, as is well-known in the art.

Farrand in view of Hirata does not disclose verifying authorization of said CPC to use said configuration data. Brosnon discloses a method of authorizing a gaming unit that is targeted to receive configuration data. This is sent by sending a signal via a data link to test the gaming unit to verify it is authorized. The gaming unit will then receive an authorization code to use the configuration data (paragraph [0060]). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Brosnon of authorizing a system to use configuration data in order to prevent users of unauthorized systems receiving configuration data.

With regard to claim 2, Farrand in view of Hirata in further view of Brosnon disclose the method of claim 1. Farrand further discloses that the data stream comprises an MPEG -4 stream (column 7, lines 14-21; Farrand establishes that the external decoder is capable of decoding "new compression" standards, including MPEG-4).

With regard to claim 4, Farrand in view of Hirata in further view of Brosnon disclose the method of claim 1 in that they disclose a decoder that is connected to a CPC with an appropriate driver. Farrand further discloses that the CPC receives the data stream (Figure 1, item 150 and column 2, lines 64-65).

Transmit said data stream to said upgrade decoder to be decoded (Figure 1, item 151 and column 3, lines 1-4).

Receive a decoded data stream from said updated decoder (Figure 1, item 151 and column 3, lines 3-5 and lines 14-16).

Claim 22 is the processor readable medium corresponding to claim 1, and is rejected as applied.

With regard to claim 24, Farrand in view of Hirata in further view of Brosnon discloses the processor readable medium of claim 22 in that they disclose detecting and accessing a removable upgrade decoder. Farrand further discloses passing a received media signal to said upgrade decoder for decoding (Figure 1, item 151). Receiving a decoded media signal from said upgrade decoder (Figure 1, item 150A) further processing said decoded media signal through traditional circuitry in said CPC (Figure 1, item 250 and column 2, line 55 – column 3, line 6; Farrand clearly discloses sending data to an upgrade module that a CPC is not capable of decoding, and receiving back a transcoded signal that the STB is capable of decoding, and then decoding the signal (item 250).

3. Claims 3 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farrand, in view of Hirata, in further view of Brosnon in further view of Garney, US Patent # 5854905, hereinafter Garney.

With regard to claim 3, Farrand in view of Hirata in further view of Brosnon discloses the method of claim 1 in that they disclose downloading a configuration data (driver) to the CPC. However, they fail to disclose a boot code program to detect the upgrade decoder and initialize the boot code program. Garney

discloses a boot support program for devices connected to a computer. Specifically, Garney discloses detecting devices and initializing them (column 3, lines 31-40; Garney describes recognizing the presence of boot devices and initializing the drivers/controllers that support these devices. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system as taught by Farrand in view of Hirata in further view of Brosnon that discloses connecting to an upgrade decoder with the feature as taught by Garney that recognizes and boots from connected devices. The advantage would have been to initialize the connection of the upgrade decoder and allow the STB to access it accordingly.

Claim 23 is the processor readable medium to perform the steps of claim 3, and is analyzed and rejected as applied.

4. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farrand, in view of Hirata in further view of Brosnon in further view of Johnson, US PG Pub # 20040223738, hereafter Johnson.

Regarding claim 5, Farrand in view of Hirata in further view of Brosnon disclose the method of claim 1 in that they disclose an upgrade decoder that increases the signal decoder capability of a CPC. However, they fail to disclose a FPGA configured to interface with the CPC.

In an analogous art, Johnson describes a system that forwards compressed data to a decoder, and uncompressed data to a receive/playback interface using an FPGA interface ([0031]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to include an FPGA to interface with a CPC such as a display device as taught by Johnson to the system taught by Farrand in view of Hirata in further view of Brosnon that interfaces a upgrade decoder to a CPC and sends compressed data between them. The advantage of this would have been to create a reliable interface at the reduced cost and complexity associated with a configurable FPGA as is known in the art.

Regarding claim 6, Farrand in view of Hirata in further view of Brosnon in further view of Johnson disclose the method of claim 5 in that they disclose an upgrade decoder that is capable of decoding signals. Farrand further discloses that the decoder is capable of decoding MPEG 4 signals (column 7, lines 14-21; Farrand establishes that the external decoder is capable of decoding "new compression" standard, including MPEG-4).

Claim 7 is rejected as applied to claim 4. As described, Farrand discloses receiving an MPEG-4 stream, which is an audio/video stream (column 3, lines 29-33) and performing the method of claim 7.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farrand, in view of Hirata, in further view of Brosnon, in further view of Johnson, in further view of Hendricks et al, US Patent # 5682195, hereafter Hendricks.

With regard to claim 8, Farrand in view of Hirata in further view of Brosnon in further view of Johnson, discloses the method of claim 7 in that they disclose transmitting an audio/video stream to an upgrade decoder from a CPC.

However, they do not disclose encrypting the data prior to transmission, or decrypting the data upon receipt.

Hendricks describes a method of delivering content in a cable television system. Specifically, he describes encrypting data prior to transmission at the head-end, and decrypting the data at an IRC upon receipt (column 12, line 66 - column 13, line 8; Hendricks specifically discloses a method of encrypting MPEG data prior to transmission and decrypting upon receipt).

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the feature of encryption/decryption to the system of Farrand in view of Hirata in further view of Brosnon in further view of Johnson that sends audio/visual content between two devices. The advantage would have been to ensure the security of the data by preventing piracy.

6. Claims 9-10, 15, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farrand, in view of Johnson, in further view of Chaney, US Patent # 5841433, hereafter Chaney.

With regard to claim 9, Farrand discloses a CPC that receives a signal (Figure 1, item 200 STB and 150 incoming data), and that contains a first signal decoder (Figure 1, item 250 and column 2, lines 60-67). Farrand further discloses that the CPC is coupled to an upgrade decoder (Figure 1, item 300, upgrade module and Figure 2 item 310 second decoder).

Farrand fails to disclose an FPGA that is coupled to the first decoder and demodulator, or a FPGA coupled to the second decoder.

In an analogous art, Johnson describes a system that forwards compressed data to a decoder, and uncompressed data to a receive/playback interface using an FPGA interface ([0031]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to include an FPGA to interface with a CPC such as a display device or a decoder as taught by Johnson to the system taught by Farrand that interfaces an upgrade decoder to a CPC and sends compressed data between them. The advantage of this would have been to create a reliable interface at the reduced cost and complexity associated with FPGA as is known in the art.

Farrand further fails to disclose a tuner and a demodulator. In an analogous art, Chaney describes a set-top-box device that comprises a tuner (Figure 7, item 734), a demodulator (Figure 7, item 735), which are coupled to an MPEG decoder (Figure 7, item 723). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to add the feature of a tuner and a demodulator to access the incoming transport stream as taught by Farrand, as is well-known in the art.

With regard to claim 10, Farrand, in view of Johnson, in further view of Chaney, discloses the CPC of claim 9 in that they disclose a CPC that receives a transport stream, and Farrand further discloses the CPC is a set-top-box (Farrand, Figure 1, item 150 and 200; Data stream and STB to receive stream).

With regard to claim 15, Farrand, in view of Johnson, in further view of Chaney disclose the CPC of claim 9 in that they disclose a device that receives media data and sends it to an upgrade decoder to be decoded. Farrand further discloses that the upgrade decoder is configured to decode MPEG-4 data (column 7, lines 14-21; Farrand establishes that the external decoder is capable of decoding "new compression" standard, including MPEG-4).

With regard to claim 17, Farrand, in view of Johnson, in further view of Chaney, disclose the CPC of claim 9 in that they disclose a device that sends coded media to an upgrade decoder to be decoded. Farrand further discloses that the upgrade decoder receives a coded data stream (Figure 1, item 151 and column 2, lines 63-67; Farrand discloses that the stream send to the upgrade decoder is encoded) and decodes said coded data stream into a data format compatible with said first signal decoder (column 3, lines 1-6; Farrand clearly discloses that the data is converted into a standard that the STB is capable of decoding).

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farrand, in view of Johnson, in further view of Chaney, in further view of Hirata, in further view of Master, US Patent # 6237029, hereinafter Master.

With regard to claim 11, Farrand, in view of Johnson, in further view of Chaney, disclose the CPC of claim 9 in that they disclose a CPC that accesses an upgrade decoder. However, they fail to disclose downloading of a configuration data to allow the CPC to access the upgrade decoder.

Hirata, in an analogous art dealing with attaching a device (in this case a printer), does disclose downloading a driver for the device via the cable head end. Such a driver, as is known in the art, would allow the STB to access the device (Figure 2, item 211 printer is attached to item 104 receiver; column 12, lines 4-7; Hirata describes downloading a driver for a device).

It would have been obvious to one of ordinary skill in the art at the time of invention to add the feature of downloading a driver to a CPC as discloses by Hirata to the system of connecting an external decoder to a CPC as taught by Farrand in view of Johnson, in further view of Chaney. The advantage would have been to allow the CPC to access the decoder properly, as is well-known in the art.

Further, Farrand, in view of Johnson, in further view of Chaney, in further view of Hirata fail to disclose the feature of an FPGA that is configured to download files, such as driver files taught by Hirata.

Master does disclose an FPGA interface that is adaptable for digital protocol processing. Specifically, he discloses an FPGA that is configured to download computer code (column 10, lines 48-55; Master discloses downloading code into a configurable FPGA).

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the feature of an FPGA interface that is configured to download code as taught by Master to the system of using code (driver) to

access an upgrade decoder device as taught by Farrand, in view of Johnson, in further view of Chaney, in further view of Hirata. The advantage would have been to use an FPGA that is configurable to the specific utility needed as is known in the art.

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farrand, in view of Johnson, in further view of Chaney, in further view of Hirata, in further view of Master in further view of Garney.

With regard to claim 12, Farrand, in view of Johnson, in view of Chaney, in further view of Master in further view of Hirata disclose the CPC of claim 11 in that they disclose a CPC with a configurable FPGA interface, however they fail to disclose the use of a boot code program to detect the decoder and initializing the boot program when the upgrade detector is connected.

Garney discloses a boot support program for devices connected to a computer. Specifically, Garney discloses detecting devices and initializing them (column 3, lines 31-40; Garney describes recognizing the presence of boot devices and initializing the drivers/controllers that support these devices. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system as taught by Farrand in view of Johnson, in further view of Chaney, in further view of Master in further view of Hirata that discloses connecting to an upgrade decoder with the feature as taught by Garney that recognizes and boots from connected devices. The advantage would have been

to initialize the connection of the upgrade decoder and allow the STB to access it accordingly.

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farrand, in view of Johnson, in further view of Chaney, in further view of Xidos et al, US Patent # 5851149, hereafter Xidos.

With regard to claim 13, Farrand, in view of Johnson, in further view of Chaney disclose the CPC of claim 9 in that they disclose a CPC with and FPGA interface to send data to the upgrade decoder for decoding. However, together, the fail to disclose that the data is locally encrypted prior to transmission, and decrypted upon receipt.

Xidos, in an analogous art, describes a set-top-box that is capable of both locally encrypting and decrypting a signal (column 36, line 65 – column 37, line 2; Xidos describes a Set-top-box that uses software to encrypt outgoing data and decrypt incoming data)

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the feature of Xidos to encrypt/decrypt outgoing/incoming data to the system of Farrand, in view of Johnson, in further view of Chaney that sends media data to an upgrade decoder for decoding. The advantage would have been to add security to the system and prevent piracy of signals.

10. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farrand, in view of Johnson, in further view of Chaney, in further view of Kurooka et al, US Patent # 6333643, hereafter Kurooka.

With regard to claim 14, Farrand, in view of Johnson, in further view of Chaney disclose the CPC of claim 9 in they disclose a CPC that has an FPGA interface configured to be coupled to an upgrade decoder, however they fail to disclose the interface comprising a hot-plug buffer configured to allow said removable upgrade decoder to be hot-swapped with the CPC.

Kurooka discloses an input/output circuit that is used for hot-plugging devices. Specifically, Kurooka describes a hot-plug buffer tolerant I/O circuit to hot-plug devices to the system (Figure 1 and column 3, lines 2-13).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to add a hot-plug tolerant buffer to the system of Farrand, in view of Johnson, in further view of Chaney that connects an upgrade decoder to an existing STB device. The advantage would have been to allow a user to plug the upgrade decoder in without re-powering the system, or to allow the user to unplug the upgrade decoder and plug in an alternate upgrade decoder without re-powering the system, or bringing the system to an unknown state.

11. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farrand, in view of Johnson, in further view of Chaney, in further view of McArthur, US Patent # 5805806.

With regard to claim 16, Farrand, in view of Johnson, in further view of Chaney disclose the CPC of claim 9 by disclosing a CPC communicatively coupled to an upgrade decoder; however they fail to specifically disclose the interface using a plurality of buffers and filters.

McArthur discloses a system that provides interactive networking between televisions and personal computers. Specifically, he discloses a TV interface that uses buffers and filters to connect to a network device (Figure 9A and item 158 buffer and 164 filter and column 9, lines 18-30; McArthur clearly discloses using buffers/filters in the interface connection). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to use buffers and amplifiers as taught by McArthur in the CPC system as taught by Farrand, in view of Johnson, in further view of Chaney. The advantage would have been to filter out undesired signals, and buffer incoming data to be decoded.

12. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farrand, in view of Johnson, in further view of Montgomery, US PG Pub # 20030161539, hereinafter Montgomery.

With regard to claim 18, Farrand discloses an upgrade decoder that contains a signal decoder that is configured to increase a signal decoding capability of a CPC. (column 2, line 55 – column 3, line 6; Farrand clearly discloses that an upgrade module is adaptive to decode a compression standard that an STB is not capable of decoding).

Farrand fails to disclose a FPGA configured to interface with a CPC.

In an analogous art, Johnson describes a system that forwards compressed data to a decoder, and uncompressed data to a receive/playback interface using an FPGA interface ([0031]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to include an FPGA to interface with a CPC such as a display device as taught by Johnson to the system taught by Farrand that interfaces an upgrade decoder to a CPC and sends compressed data between them. The advantage of this would have been to create a reliable interface at the reduced cost and complexity associated with a configurable FPGA as is known in the art.

Farrand in view of Johnson fails to disclose an encryption/decryption engine, comprised within the upgrade decoder, configured to locally encrypt and decrypt audio/video signals. Montgomery discloses a digital storage system in a distributed surveillance system. In figure 1, Montgomery illustrates cameras 110-1 - 100-n connected to computers 120-1 - 120-n. In paragraph [0012]; Montgomery discloses that each camera can have its own computer or multiple cameras can be grouped together to one computer. The computers are connected to central servers 140-1 - 140-n (Figure 1 and paragraph [0012]). In Figure 2, Montgomery illustrates that an encryption/decryption module 210-4 is resident in the local computer, which is further described in paragraphs [0019 and 0023]. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Montgomery to include

the local encryption/decryption module within the local computer to locally encrypt and decrypt signals, with the advantage of potential cost and space savings without the need of an additional piece of hardware.

With regard to claim 19, Farrand in view of Johnson in further view of Montgomery teach the upgrade decoder of claim 18 in that they teach a device that upgrades the capability of an existing set-top-box. Further, Farrand describes that the module is connected via a USB or P1394 interface (column 3, lines 53-63) corresponding to the module being removable from the system. In contrast, Farrand describes an embodiment (Figure 4) in which the extra decoder is not removable, rather part of the STB.

With regard to claim 20, Farrand, in view of Johnson in further view of Montgomery teach the upgrade decoder of claim 18 they teach a device that upgrades the capability of an existing set-top-box. Farrand further discloses that the upgrade decoder is configured to decode MPEG-4 data (column 7, lines 14-21; Farrand establishes that the external decoder is capable of decoding "new compression" standard, including MPEG-4).

13. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farrand, in view of Johnson in further view of Kurooka.

With regard to 21, Farrand, in view of Johnson disclose the upgrade decoder of claim 18 by disclosing an upgrade decoder connected to a CPC via a

configurable FPGA interface, however they fail to disclose a hot-plug buffer configured to allow said upgrade decoder to be hot-swapped with said CPC.

Kurooka discloses an input/output circuit that is used for hot-plugging devices. Specifically, Kurooka describes a hot-plug buffer tolerant I/O circuit to hot-plug devices to the system (Figure 1 and column 3, lines 2-13).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to add a hot-plug tolerant buffer to the system of Farrand in view of Johnson that connects an upgrade decoder to an existing STB device. The advantage would have been to allow a user to plug the upgrade decoder in without re-powering the system, or to allow the user to unplug the upgrade decoder and plug in an alternate upgrade decoder without re-powering the system, or bringing the system to an unknown state.

14. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farrand, in view of Hirata, in further view of Brosnon in further view of Hendricks.

With regard to claim 25, Farrand in view of Hirata in further view of Brosnon disclose the processor readable medium of claim 24 in that they disclose a CPC that sends data to an upgrade decoder for decoding. However, they fail to disclose the feature of encrypting the signal prior to passing the signal to the upgrade decoder.

Hendricks describes a method of delivering content in a cable television system. Specifically, he describes encrypting data prior to transmission at the

head-end, and decrypting the data at an IRC upon receipt (column 12, line 66 - column 13, line 8; Hendricks specifically discloses a method of encrypting MPEG data prior to transmission and decrypting upon receipt).

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the feature of encryption/decryption to the system of Farrand in view of Hirata in further view of Brosnon that sends audio/visual content between two devices. The advantage would have been to ensure the security of the data by preventing piracy.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARK D. FEATHERSTONE whose telephone number is (571)270-3750. The examiner can normally be reached on 8:00 AM - 5:00 PM M-F US Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Koenig can be reached on (571) 272-7296. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

E-Signed

/Mark Featherstone/ - Assistant Examiner

/Andrew Y Koenig/
Supervisory Patent Examiner, Art Unit 2423